# PhotonHub Experience Centre

## Silicon and Silicon Nitride Photonic Integrated Circuits

## Course Provider

ePIXfab – the European Silicon Photonics Alliance
and its members
Hosted from Ghent University, Belgium

# Course Overview

Silicon photonics (SiPh) is a key photonic integration technology. The evolution pace of silicon photonics technology is tremendous. Industries developing SiPh-based solutions have to continuously train their workforce to equip them with latest trends and developments.

This 3-day training course provides industry, especially those involved in PIC-based product development, with the basic technical skills in ideating, designing, fabricating and testing SiPh PICs. The course covers various forms of SiPh such as thin SOI, thick SOI, LPCVD SiN, PECVD SiN, and Ge- on-Si along with the deployment of these technologies into application domains such as communications, medical, sensors, quantum, environmental, computing, etc.

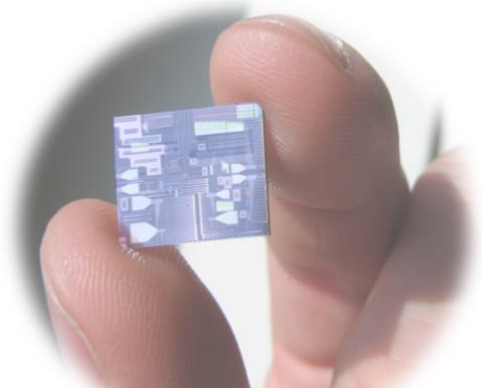
The training will be organized by ePIXfab (hosted by UGent) with the support of its members that are partners in PhotonHub Europe project. The support provided by ePIXfab members will make the course cohesive and inclusive to all forms and brands of SiPh technologies – that is the biggest value proposition of the proposed course and makes it unique in the European landscape.

The training will provide a hands-on training with respect to:

- determining the right SiPh technology platform & design environment for a given application
- designing a SiPh chip and associated key fabrication steps
- developing test-beds and testing of SiPh PICs for various applications.

# Target Audience

It is desirable but not essential that course attendees have a basic understanding of photonics. The course is ideally suited to those planning to internalize basic skills necessary for innovative PIC-based product development.



# Expected Outcomes

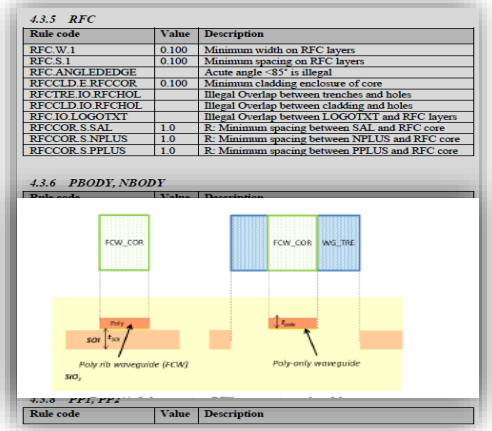
1) Mastery in choosing the appropriate technology platform for a use case
2) Mastery in adopting the right design framework for a use case
3) Hands-on skills with respect to the SiPh design process
4) Understanding of challenges associated with the fabrication of SiPh chips
5) Experience in different testing schemes and fiber-chip-fiber coupling schemes
6) Experience in on-chip opto-electronic testing, including high speed testing

# Difficulty Level

The training is designed for newcomers to the field of silicon photonics. The training touches all elements of silicon photonics prototyping without going into an extreme level of detail.

# Course Equipment & Infrastructure

Design Software
(Device, Circuit, Layout, System)



4.3.5 RFC

| Rule code | Value | Description |
|---|---|---|
| RFC.W.1 | 0.100 | Minimum width on RFC layers |
| RFC.S.1 | 0.100 | Minimum spacing on RFC layers |
| RFC.ANGLEDEDGE | | Acute angle <85° is illegal |
| RFCCLD.E.RFCCOR | 0.100 | Minimum cladding enclosure of core |
| RFCTRE.IO.RFCHOL | | Illegal Overlap between trenches and holes |
| RFCCLD.IO.RFCHOL | | Illegal Overlap between cladding and holes |
| RFC.IO.LOGOTXT | | Illegal Overlap between LOGOTXT and RFC layers |
| RFCCOR.S.SAL | 1.0 | R: Minimum spacing between SAL and RFC core |
| RFCCOR.S.NPLUS | 1.0 | R: Minimum spacing between NPLUS and RFC core |
| RFCCOR.S.PPLUS | 1.0 | R: Minimum spacing between PPLUS and RFC core |

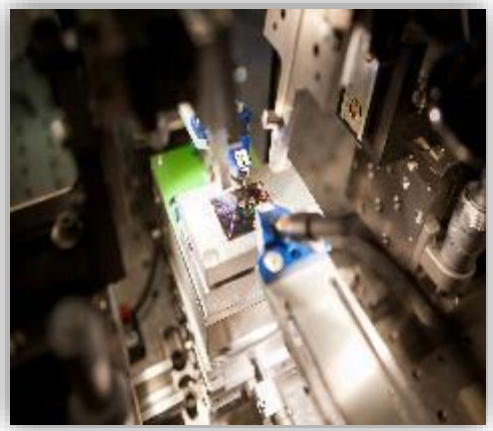
4.3.6 PBODY, NBODY



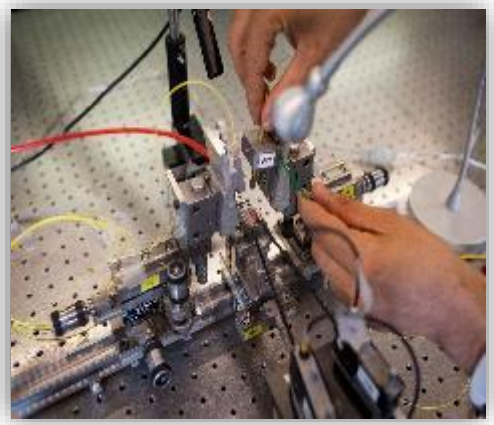
| Rule code | Value | Description |
|---|---|---|

Fab-like PDKs

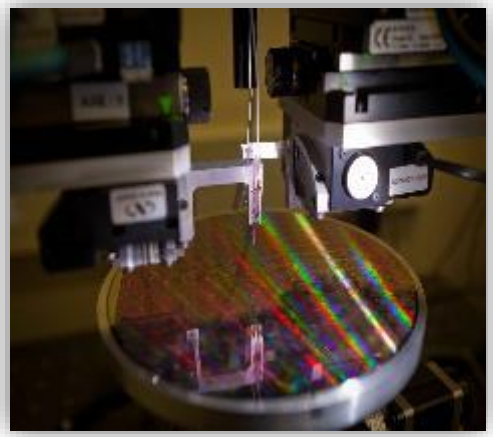
Cleanroom processes



High-speed test beds



Vertical and horizontal coupling setups



Wafer-level automated testing setups

# Course Schedule

| Day | Time | Training Activity |
|---|---|---|
| DAY 1<br><br>Wednesday,<br>10 May 2023 | 09:00 – 10:00 | Welcome, Housekeeping, short introduction to silicon photonics |
| | 10:00 – 12:30 | Learn how to design photonic integrated circuits (PICs) for silicon photonics – Part 1 (Hands-on) |
| | 12:30 – 17:00 | Learn how to design photonic integrated circuits (PICs) for silicon photonics – Part 2 (Hands-on) |
| DAY 2<br><br>Thursday,<br>11 May 2023 | 09:00 – 10:00 | Learn how a chip is made (tutorial) |
| | 10:30 – 12:30 | Learn about silicon photonics platforms in relation to application areas (hands-on) |
| | 13:30 – 17:00 | e-beam writing of the design + reactive ion etching (hands-on) |
| | 19:00 – 20:30 | Learn about light source co-integration (tutorials) |
| DAY 3<br><br>Friday,<br>12 May 2023 | 09:00 – 12:30 | Learn to couple light into a chip from a fiber for different application wavelengths (demos + hands-on) |
| | 13:30 – 17:00 | Learn to test an unpackaged silicon/silicon nitride PICs for various application areas (demos + hands-on) |
| | 17:30 – 18:30 | Digital meetup and Q&A with fab experts (online) |

# Program: Day 1

**Module:**
**Learn how to design a silicon photonic integrated circuit**

**Tutors:**


Prof. Roel Baets


Dr. Abdul Rahim


Prof. Wim Bogaerts


Dr. Umar Khan

| Element | Speaker/Trainer | Where? | When? |
|---|---|---|---|
| Welcome | Roel Baets | Room Allan Turing , iGent Tower, Floor 1 | 09:00 – 09:10 |
| Program and Housekeeping | Abdul Rahim | | 09:10 - 09:20 |
| Short introduction to silicon photonics | Wim Bogaerts | | 09:20 – 10:00 |
| Tutorial:<br>• Concept of process design kit (PDK)<br>• How to design silicon photonic ICs?<br>• Compact models and circuit simulations | Umar Khan | | 10:00 – 10:30 |
| Hands-on:<br>Designing a simple silicon photonic IC | Umar Khan | | 10:30 – 12:30 |
| Hands-on:<br>Designing a simple silicon photonic IC | Umar Khan | | 1:30 – 5:15 |
| Quiz | Umar Khan | | 5:15 – 5:30 |

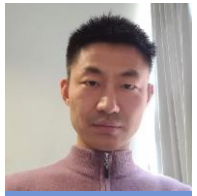
Available in the meeting room

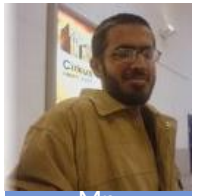
12:30 – 1:30 PM at Floor 12 of iGent Building

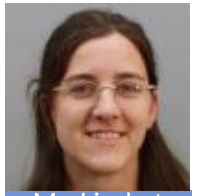
# Program: Day 2

**Module:**
**Learn how to design a silicon photonic integrated circuit**

**Tutors:**


Dr. Dongbo Wang


Mr. Muhammad Muneeb


Ms. Liesbet Van Landschoot


Prof. Gunther Roelkens

| Element | Speaker/Trainer | Where? | When? |
|---|---|---|---|
| Tutorial:<br>Overview of silicon photonics chip fabrication in a CMOS fab | Dongbo Wang | Room Allan Turing , iGent Tower, Floor 1 | 09:00 – 10:00 |
| Demos:<br>• Clean room safety<br>• Exposure to different silicon photonics platforms | Muhammad Muneeb | Tech. Park building 123<br>(Clean room building) | 10:30 – 12:00 |
| Hands-on:<br>• Sample preparation (cleaving, cleaning, spin-coating)<br>• E-beam exposure of the design from Day 1<br>• Reactive ion etching of the exposed and developed samples | Muhammad Muneeb, Dongbo Wang, Liesbet Van Landschoot | Tech. Park building 123<br>(Clean room building) | 1:00 – 4:30 |
| Tutorial:<br>Laser co-integration with silicon photonics | Gunther Roelkens | Room Allan Turing , iGent Tower, Floor 1 | 5:00 – 6:00 |
| Quiz | | | 6:00 – 6:15 |
| Group Dinner | | In a local Ghent Restaurant | 7 PM – 10 PM |

Available in the meeting room

12:30 – 1:30 PM at Floor 12 of iGent Building

# Program: Day 3

**Module:**
**Learn how to characterize a silicon PICs**

**Tutors:**


Dr. Jing Zhang


Mr. Ewoud Vissers


Mr. Hong Deng


Dr. Maximilien Billet


Dr. Laurens Bogaert

| Element | Speaker/Trainer | Where? | When? |
|---|---|---|---|
| Hands-on:<br>• Execute and optimize coupling of light in and out of a chip, both horizontally and vertically (single fiber or fiber array) for different application wavelengths<br>  • Execute the measurement of a simple silicon photonic circuit (e.g., a ring resonator or an MZI)<br>  • Test a PIC with optical and low-speed electrical probing (for example, by thermal heaters) | Jing Zhang, Ewoud Vissers, Hong Deng | Measurement rooms, iGent Tower, Floor 4 | 09:00 – 12:30 |
| Hands on:<br>• Test a PIC with optical and high-speed electrical probing<br>• Characterization of a laser integrated on a silicon photonics chip | Laurens Bogaert, Maximilien Billet | Measurement rooms, iGent Tower, Floor 4 | 1:30 – 4:30 |
| Demo:<br>• analyze the measured data for chip fabricated on Day 2 | Umar Khan | Measurement rooms, iGent Tower, Floor 4 | 4:30 – 5:00 |
| Quiz | | | 5:00 – 5:15 |

Available in the meeting room  12:30 – 1:30 PM at Floor 12 of iGent Building

# Course Trainers

**Course Directors:** Prof. Roel Baets, Prof. Wim Bogaerts

**Course Manager:** Dr. Abdul Rahim

**Tutorials:** Selected speakers from PhotonHub , Experts from UGent- ePIXfab

**Chip Fabrication:** UGent Cleanroom staff

**Chip Coupling:** ePIXfab + UGent Manpower + Application engineers from PhotonHub partners

**Chip Testing:** ePIXfab + UGent Manpower + Application engineers from PhotonHub partners

# **Course Material** (technical hand-outs)


https://einstein.epixfab.eu

- Electronic access to
  - Course handouts/slides
  - Video recordings of tutorials
  - Design examples
  - Python notebooks
  - Video recordings of lab demos

# Course Location, Schedule & Cost

- Course Location: Ghent, Belgium
- Course Schedule (exact dates to be confirmed)
- Number of people (Groups of 10 people per course)
- Course Cost (500 Euros per person, includes lunch catering, handouts, etc.)

# Further Information

- abdul.rahim@epixfab.eu
- https://epixfab.eu
- www.photonhub.eu/euphotonicsacademy

UGent
Cleanroom

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9052 Gent

At the heart
of Europe

# Keywords

Silicon photonics, SOI, Silicon Nitride, High Index Contrast, CMOS, Laser, Modulators, Detectors, Component design, Circuit simulation, System emulation, Design layout, Design Rules, Manufacturing, Pilot Line, Ecosystem, Open-access, Fabless, Fab-lite, Communications, Medical, Sensors, Quantum, Environmental, Computing